09-06-00

Practitioner's Docket No. 297-009750-US(PAR) **PATENT**

Preliminary Classification:
Proposed Class:
Subclass:

NOTE: "All applicants are requested to include a preliminary classification on newly filed patent applications. The preliminary classification, preferably class and subclass designations, should be identified in the upper right-hand corner of the letter of transmittal accompanying the application papers, for example 'Proposed Class 2, subclass 129.'" M.P.E.P. § 601, 7th ed.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Esa HARMA, Jouko HAKKANEN

WARNING: *37 C.F.R. § 1.41(a)(1) points out:*

"(a) A patent is applied for in the name or names of the actual inventor or inventors.

"(1) The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.63, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors."

For (title): SERIAL INTERFACE AND METHOD FOR TRANSFERRING DIGITAL DATA OVER A SERIAL INTERFACE

CERTIFICATION UNDER 37 C.F.R. § 1.10*
(Express Mail label number is mandatory.)
(Express Mail certification is optional.)

I hereby certify that this New Application Transmittal and the documents referred to as attached therein are being deposited with the United States Postal Service on this date 5 September 2000, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EL627420396US, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Elaine Mian
(type or print name of person mailing paper)

Elaine Mian
Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. § 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

WARNING: *Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. § 1.10(b).*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Type of Application

This new application is for a(n)

(check one applicable item below)

- ☒ Original (nonprovisional)
- ☐ Design
  - ☐ Plant

WARNING: ***Do not*** *use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. § 371(c)(4), unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: ***Do not*** *use this transmittal for the filing of a provisional application.*

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

- ☐ Divisional.
- ☐ Continuation.
- ☐ Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. §§ 119(e), 120, or 121)

NOTE: A nonprovisional application may claim an invention disclosed in one or more prior filed copending nonprovisional applications or copending international applications designating the United States of America. In order for a nonprovisional application to claim the benefit of a prior filed copending nonprovisional application or copending international application designating the United States of America, each prior application must name as an inventor at least one inventor named in the later filed nonprovisional application and disclose the named inventor's invention claimed in at least one claim of the later filed nonprovisional application in the manner provided by the first paragraph of 35 U.S.C. § 112. Each prior application must also be:

(i) An international application entitled to a filing date in accordance with PCT Article 11 and designating the United States of America; or

(ii) Complete as set forth in § 1.51(b); or

(iii) Entitled to a filing date as set forth in § 1.53(b) or § 1.53(d) and include the basic filing fee set forth in § 1.16; or

(iv) Entitled to a filing date as set forth in § 1.53(b) and have paid therein the processing and retention fee set forth in § 1.21(l) within the time period set forth in § 1.53(f).

37 C.F.R. § 1.78(a)(1).

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. §§ 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. §§ 120, 121 or 365(c). (35 U.S.C. § 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. §§ 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

WARNING: *When the last day of pendency of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, any nonprovisional application claiming benefit of the provisional application must be filed prior to the Saturday, Sunday, or Federal holiday within the District of Columbia. See 37 C.F.R. § 1.78(a)(3).*

☐ The new application being transmitted claims the benefit of prior U.S. application(s). Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for filing date under 37 C.F.R. § 1.53(b) (Regular) or 37 C.F.R. § 1.153 (Design) Application

16 Pages of specification

4 Pages of claims

9 Sheets of drawing

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. For comments on proposed then-new 37 C.F.R. § 1.84, see Notice of March 9, 1988 (1990 O.G. 57-62).*

NOTE: "Identifying indicia, if provided, should include the application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application. This information should be placed on the back of each sheet of drawing a minimum distance of 1.5 cm. (5/8 inch) down from the top of the page . . ." 37 C.F.R. § 1.84(c)).

(complete the following, if applicable)

☐ The enclosed drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. § 1.84(b).

☐ formal

☐ informal

B. Other Papers Enclosed

6 Pages of declaration and power of attorney

1 Pages of abstract

____ Other

4. Additional papers enclosed

☐ Amendment to claims

☐ Cancel in this applications claims _____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

☐ Add the claims shown on the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims.)

☐ Preliminary Amendment

☒ Information Disclosure Statement (37 C.F.R. § 1.98)

☒ Form PTO–1449 (PTO/SB/08A and 08B)

☒ Citations

- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☐ Other

5. Declaration or oath (including power of attorney)

NOTE: A newly executed declaration is not required in a continuation or divisional application provided that the prior nonprovisional application contained a declaration as required, the application being filed is by all or fewer than all the inventors named in the prior application, there is no new matter in the application being filed, and a copy of the executed declaration filed in the prior application (showing the signature or an indication thereon that it was signed) is submitted. The copy must be accompanied by a statement requesting deletion of the names of person(s) who are not inventors of the application being filed. If the declaration in the prior application was filed under § 1.47, then a copy of that declaration must be filed accompanied by a copy of the decision granting § 1.47 status or, if a nonsigning person under § 1.47 has subsequently joined in a prior application, then a copy of the subsequently executed declaration must be filed. See 37 C.F.R. §§ 1.63(d)(1)–(3).

NOTE: A declaration filed to complete an application must be executed, identify the specification to which it is directed, identify each inventor by full name including family name and at least one given name, without abbreviation together with any other given name or initial, and the residence, post office address and country or citizenship of each inventor, and state whether the inventor is a sole or joint inventor. 37 C.F.R. § 1.63(a)(1)–(4).

☒ Enclosed

Executed by

(check **all** *applicable boxes)*

- ☒ inventor(s).
- ☐ legal representative of inventor(s).
  37 C.F.R. §§ 1.42 or 1.43.
- ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
  - ☐ This is the petition required by 37 C.F.R. § 1.47 and the statement required by 37 C.F.R. § 1.47 is also attached. *See* item 13 below for fee.

☐ Not Enclosed.

NOTE: Where the filing is a completion in the U.S. of an International Application or where the completion of the U.S. application contains subject matter in addition to the International Application, the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

☐ Application is made by a person authorized under 37 C.F.R. § 1.41(c) on behalf of *all* the above named inventor(s).

(The declaration or oath, along with the surcharge required by 37 C.F.R. § 1.16(e) can be filed subsequently).

☐ Showing that the filing is authorized.
(not required unless called into question. 37 C.F.R. § 1.41(d))

6. Inventorship Statement

WARNING: *If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.*

The inventorship for all the claims in this application are:

☐ The same.

or

☐ Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,

☐ is submitted.

☐ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. An English translation of the non-English language application and the processing fee of $130.00 required by 37 C.F.R. § 1.17(k) is required to be filed with the application, or within such time as may be set by the Office. 37 C.F.R. § 1.52(d).

☒ English

☐ Non-English

☐ The attached translation includes a statement that the translation is accurate. 37 C.F.R. § 1.52(d).

8. Assignment

☒ An assignment of the invention to Nokia Mobile Phones Ltd.

☒ is attached. A separate ☒ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☐ FORM PTO 1595 is also attached.

☐ will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment." Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "CERTIFICATE UNDER 37 C.F.R. § 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993, 1150 O.G. 62-64.*

9. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. No.	Filed
Finland	19991900	6 September 1999
Country	Appln. No.	Filed
Country	Appln. No.	Filed

from which priority is claimed

☒ Is (are) attached.

☐ Will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 C.F.R. § 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. § 120 is itself entitled to priority from a prior foreign application, then complete Item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. § 1.16)

A. ☒ Regular application

CLAIMS AS FILED

Number filed		Number Extra		Rate	Basic Fee 37 C.F.R. § 1.16(a) $ 690.00
Total Claims (37 C.F.R. § 1.16(c))	18 − 20 =	0	×	$ 18.00	0
Independent Claims (37 C.F.R. § 1.16(b))	4 − 3 =	1	×	$ 78.00	78.00
Multiple dependent claim(s), if any (37 C.F.R. § 1.16(d))			+	$260.00	

☐ Amendment cancelling extra claims is enclosed.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 C.F.R. § 1.16(d).

Filing Fee Calculation $ 768.00

B. ☐ Design application ($310.00—37 C.F.R. § 1.16(f))

Filing Fee Calculation $_____

C. ☐ Plant application ($480.00—37 C.F.R. § 1.16(g))

Filing fee calculation $_____

11. Small Entity Statement(s)

☐ Statement(s) that this is a filing by a small entity under 37 C.F.R. § 1.9 and 1.27 is (are) attached.

WARNING: "Status as a small entity must be specifically established in each application or patent in which the status is available and desired. Status as a small entity in one application or patent does not affect any other application or patent, including applications or patents which are directly or indirectly dependent upon the application or patent in which the status has been established. The refiling of an application under § 1.53 as a continuation, division, or continuation-in-part (including a continued prosecution application under § 1.53(d)), or the filing of a reissue application requires a new determination as to continued entitlement to small entity status for the continuing or reissue application. A nonprovisional application claiming benefit under 35 U.S.C. § 119(e), 120, 121, or 365(c) of a prior application, or a reissue application may rely on a statement filed in the prior application or in the patent if the nonprovisional application or the reissue application includes a reference to the statement in the prior application or in the patent or includes a copy of the statement in the prior application or in the patent and status as a small entity is still proper and desired. The payment of the small entity basic statutory filing fee will be treated as such a reference for purposes of this section." 37 C.F.R. § 1.26(a)(2).

*WARNING: "Small entity status must not be established when the person or persons signing the . . . statement can **unequivocally** make the required self-certification." M.P.E.P., § 509.03, 6th ed., rev. 2, July 1996 (emphasis added).*

(complete the following, if applicable)

☐ Status as a small entity was claimed in prior application _____ / _____, filed on _____, from which benefit is being claimed for this application under:

35 U.S.C. § ☐ 119(e),
☐ 120,
☐ 121,
☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the statement in the prior application is included.

Filing Fee Calculation (50% of **A, B** or **C** above)

$_____

NOTE: Any excess of the full fee paid will be refunded if small entity status is established and a refund request are filed within 2 months of the date of timely payment of a full fee. The two-month period is not extendable under § 1.136. 37 C.F.R. § 1.26(a).

12. Request for International-Type Search (37 C.F.R. § 1.104(d))

(complete, if applicable)

☐ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. § 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Filing fee $ 768.00

☒ Recording assignment ($40.00; 37 C.F.R. § 1.21(h)) (See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) $ 40.00

☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached ($130.00; 37 C.F.R. §§ 1.47 and 1.17(i)) $ _____

☐ For processing an application with a specification in a non-English language ($130.00; 37 C.F.R. §§ 1.52(d) and 1.17(k)) $ _____

☐ Processing and retention fee ($130.00; 37 C.F.R. §§ 1.53(d) and 1.21(l)) $ _____

☐ Fee for international-type search report ($40.00; 37 C.F.R. § 1.21(e)) $ _____

NOTE: 37 C.F.R. § 1.21(l) establishes a fee for processing and retaining any application that is abandoned for failing to complete the application pursuant to 37 C.F.R. § 1.53(f) and this, as well as the changes to 37 C.F.R. §§ 1.53 and 1.78(a)(1), indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid, or the processing and retention fee of § 1.21(l) must be paid, within 1 year from notification under § 53(f).

Total fees enclosed $ 808.00

14. Method of Payment of Fees

☒ Check in the amount of $ 808.00

☐ Charge Account No. _____ in the amount of $_____.

A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 C.F.R. § 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: If no fees are to be paid on filing, the following items should not be completed.

WARNING: Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.

☒ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 16-1350 :

☒ 37 C.F.R. § 1.16(a), (f) or (g) (filing fees)

☒ 37 C.F.R. § 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

☒ 37 C.F.R. § 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

☒ 37 C.F.R. § 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a)).

☐ 37 C.F.R. § 1.17 (application processing fees)

NOTE: ". . .A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

☐ 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b).

NOTE: 37 C.F.R. § 1.28(b) requires "Notification of any change in status resulting in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying, . . . the issue fee. . . " From the wording of 37 C.F.R. § 1.28(b), (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions as to Overpayment

NOTE: ". . . Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

☒ Credit Account No. 16-1350

☐ Refund

SEND ALL CORRESPONDENCE TO:

Clarence A. Green (Reg. No.: 24,622)
PERMAN & GREEN, LLP
425 Post Road
Fairfield, Connecticut 06430

Reg. No. 42,841

Tel. No. (203) 259-1800

Customer No. 2512

SIGNATURE OF PRACTITIONER

Janik Marcovici

(type or print name of attorney)

PERMAN & GREEN, LLP

P.O. Address

425 Post Road, Fairfield, Connecticut 06430

☐ **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

☐ Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added _____

☐ Plus Added Pages for Papers Referred to In Item 4 Above

Number of pages added _____

☐ Plus added pages deleting names of inventor(s) named in prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added _____

☐ Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

☒ **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

☒ This transmittal ends with this page.

TITLE: Serial interface and method for transferring digital data over a serial interface

TECHNOLOGICAL FIELD

The invention concerns generally the technology of transferring structured digital data over a wired connection. Especially the invention concerns the technology of encoding the synchronization information needed for maintaining the structures of the digital data in a wired serial interface.

BACKGROUND OF THE INVENTION

For transferring digital data between circuit elements the basic approaches of parallel and serial interfacing are available. A parallel interface consists of a number of parallel wired connections or lines so that a number of bit values may be transferred simultaneously by setting either the logical value "1" or the logical value "0" to each line, i.e. either setting or resetting each line simultaneously. A serial interface does not necessarily involve more than one data line on which the bit values are transferred sequentially by repeatedly either setting or resetting the data line.

The situation gets somewhat more complicated if the signal to be transmitted must conform to a certain higher-level structure, meaning that there are relatively long data sequences that must be handled independently from each other. In this patent application we will especially describe the transmission of digital image data over an interface. A digital image consists nearly always of a rectangular array of elementary picture elements or pixels. The image is read by scanning the horizontal lines formed by adjacent pixels in a prescribed order, usually from top to down and from left to right. In the resulting digital bit stream a predetermined number of bits describes the color of each pixel, the beginning of a line is indicated by a certain line synchronization or LSYNC signal and the beginning of a new image frame is indicated by a certain frame synchronization or FSYNC signal.

In order for the image transmission to function properly the transmitting device and the receiving device must share a common clock frequency for writing on and reading from the interfacing lines. Additionally the transmitting device must

correctly convey the LSYNC and FSYNC signals to the receiving device in one way or another.

Fig. 1 illustrates a conventional parallel interface between a transmitting device 101 and a receiving device 102. The interface consists of a number of data lines, which are here numbered from 1 to N, a number of control lines and a clock line CLK. The number of control lines is shown to be M, and because we discuss especially the transmission of digital image data, among the control lines there are the synchronization lines FSYNC and LSYNC.

Fig. 2a illustrates schematically how the interface between devices 101 and 102 may be "serialized". A parallel to serial (P/S) converter 201 is coupled to the parallel output of the transmitting device 101, and a corresponding serial to parallel (S/P) converter is coupled to the parallel input of the receiving device 102. A phase locked frequency multiplier 203 is utilized to multiply the frequency of the clock signal CLK coming from the transmitting device by N+M. The basic clock frequency CLK drives the parallel side of the P/S converter 201 and its N+M-multiplied version drives the serial side. Correspondingly a frequency divider 204 is used to restore the original CLK frequency at the receiving end so that the received N+M-multiplied clock frequency drives the serial side of the S/P converter and the original CLK frequency drives the parallel side. The original CLK frequency is also provided to the receiving device 102 for synchronizing the reading of the parallel input data. In addition to just converting the interface into serial form Fig. 2a illustrates how the immunity of the data and clock lines against common-mode interference may be enhanced by using differential transmitter-receiver pairs 205, 206 and 207, 208 respectively. For short differential transmission links e.g. between two integrated circuits within a single electronic apparatus it is commonplace to use so-called low-level differential transmitters and receivers so that the differential voltage levels appearing in the serial connection are well under the conventional +5V...-5V levels.

Fig. 2b illustrates the basic serial interface model where a transmitting device 251 needs only one connection to the receiving device 252. The transmitting device 251 comprises a multiplexer 253 that multiplexes the bits of the DATA, LSYNC and FSYNC digital signals into a common connecting line in the pace determined by a clock signal CLK. In the receiving device 252 there is a corresponding demultiplexer 254. In Fig. 2b the actual wired connection between the transmitting end and the receiving end is also shown to be differential, utilizing the differential

transmitter 255 and the differential receiver 256. The LSYNC and FSYNC bit sequences that are multiplexed into the common connection must consist of bit patterns that are long enough so that their composition can be selected to be unique: when the demultiplexer 254 recognizes a certain predetermined pattern of consecutive bits in the received bitstream, it indicates that a synchronization signal has been received. We may refer to a number of consecutive bits as N, and denote the number of synchronization bits constituting the LSYNC and FSYNC patterns therein as M.

If the clock frequency of an interface is kept constant and not converted to higher values, a parallel interface is more effective in terms of throughput since N+M bits are transferred on each cycle of the basic clock frequency CLK. However, modern VLSI (Very Large Scale Integration) technology has made it possible to integrate so many different functions on a single semiconductor chip that the number of input and output lines to and from the chips has become a limiting factor. Serial interfaces do not need even nearly as many lines as parallel ones, which makes serializing an important aspect in modern circuit design.

The drawback of the arrangements of Figs. 2a and 2b is that for a fraction M / (N+M) of the time the serial interfacing line is not transferring actual data or payload information, since it is used for transmitting control information. For example in Fig. 2a a feasible choice for values of M and N in practice could be M= 2 and N=8, which would mean that only 80% of the active communication time is used for transmitting actual data. An additional drawback is the relatively high clock frequency, N+M times CLK, which is required to operate the converters and to time the transmission over the serial line(s). Usually the power consumption of converter devices is directly proportional to their operating frequency, and especially in small-sized portable electronic apparatuses all power consumption should be kept at minimum. Additionally a high clock frequency in a serial interface increases the amount of electromagnetig interference (EMI) caused to the surrounding circuitry.

The arrangements of Figs. 2a and 2b is also susceptible to synchronization errors. The S/P converter in Fig. 2a is basically a parallel array of memory locations. A bit value is read from the serial line at each cycle of the multiplied clock frequency and written into a certain memory location. At the next cycle of the basic CLK frequency the data in the memory locations is latched into the parallel lines. If the writing started from an incorrect memory location, or if a distortion in the multiplied clock frequency line somehow erased one or more cycles of the multiplied clock

frequency, the receiver may not get a correct result. The same applies if a bit is lost or inverted in the synchronization patterns required by the solution of Fig. 2b.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method and an arrangement for conveying control information over a serial interface with a better efficiency in communication time utilization than in the described prior art arrangements. It is a further object of the invention to provide a serial interface arrangement with lower power consumption than in the described prior art arrangements. An even further object of the invention is to provide a method and an arrangement for conveying control information over a serial interface with less EMI being caused. An additional object of the invention is to provide a method and an arrangement for conveying control information over a serial interface with less susceptibility to synchronization errors.

The objects of the invention are achieved by defining several signal levels to be used in the serial interface and by allocating distinctive signal levels for actual data and control information.

A serial interface transmitter according to the invention is characterized in that it comprises

- primary transmitter means for converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels and
- secondary transmitter means for converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

A serial interface receiver according to the invention is characterized in that it comprises

- primary receiver means, responsive to a first group of signal levels, for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits and

- secondary receiver means, responsive to a second group of signal levels which consists of different levels than said first group of signal levels, for converting synchronization signal levels in said input line into synchronization signals.

An electronic device according to the invention comprises a first circuit element and a second circuit element for processing digital image data consisting of data sequences and synchronization signals. It is characterized in that it comprises within the first circuit element a digital transmitting device of the above-mentioned kind and within the second circuit element a digital receiving device of the above-mentioned kind.

The invention also applies to a method which is characterized in that it comprises the steps of

- converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels, and
- converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

According to the invention the transmitter and receiver sides of the serial part of an interface are designed so that several distinctive set levels are allowed on the serial line(s). At least one of the set levels is used to transmit the set values belonging to the actual information, and at least one other set level is used to superimpose the control information onto the actual information.

A piece of control information may be transmitted on the serial line without a data bit value being sent simultaneously. In this case the transmission of data has to be interrupted for the time it takes to transmit the piece of control information, and the level and/or polarity of the piece of control information indicates which value the control information has and how it should be interpreted at the receiving end. However, if sufficient resolution is provided at the receiving end, a piece of control information may be transmitted even simultaneously with a piece of actual data, in which case the receiver measures a received level on the serial line and separates from the measurement the control information part and the actual information part.

BRIEF DESCRIPTION OF DRAWINGS

The novel features which are considered as characteristic of the invention are set forth in particular in the appended Claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Fig. 1 illustrates a known parallel interface,
Fig. 2a illustrates a known serialized parallel interface,
Fig. 2b illustrates a known serial interface,
Fig. 3 illustrate the principle of the invention,
Fig. 4 illustrates an apparatus according to a first embodiment of the invention,
Fig. 5a illustrates a first part of a timing diagram relating to Fig. 4,
Fig. 5b illustrates a second part of a timing diagram relating to Fig. 4,
Fig. 6 illustrates an apparatus according to a second embodiment of the invention,
Fig. 7a illustrates a first part of a timing diagram relating to Fig. 6,
Fig. 7b illustrates a second part of a timing diagram relating to Fig. 6,
Fig. 8 illustrates an apparatus according to a third embodiment of the invention,
Fig. 9a illustrates a voltage level diagram relating to Fig. 8,
Fig. 9b illustrates a first part of a timing diagram relating to Fig. 8,
Fig. 9c illustrates a second part of a timing diagram relating to Fig. 8,
Fig. 10 illustrates an apparatus according to a fourth embodiment of the invention and
Fig. 11 illustrates a voltage level diagram relating to Fig. 10.

Similar parts in the drawings are denoted with same reference designators.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 3 illustrates a serial interfacing principle where a transmitting device 301 is coupled to a receiving device 302 through a wired serial connection. The arrangement is meant to enable the transmission of such digital data where regularly occurring synchronization signals of one or more type divide the data bit stream into subsequent blocks, such as lines and/or frames of digital image data. The transmitting device 301 comprises means 303 for converting the data bit stream with its associated synchronization signals to be transmitted into a signal where a certain first signal level or a certain first set of signal levels are used to indicate the

transmitted data bit values and a certain second signal level or a certain second set of signal levels are used to indicate the occurrence and/or type of the synchronization signals. Correspondingly the receiving device 302 comprises means 304 for converting the observed signal levels in a received signal into a data bit stream and its associated synchronization signals so that a certain first observed signal level or a certain first set of observed signal levels are used to reconstruct the transmitted data bit values and a certain second observed signal level or a certain second set of observed signal levels are used to reconstruct the occurrence and/or type of the synchronization signals. The levels refer most commonly to voltage levels, but they may also refer to current levels or the levels of some other measurable quantity.

Fig. 4 is a more detailed schematic diagram of a first practical embodiment of the invention. In the transmitting device there is a DATA line carrying a serial data bit stream consisting of the electrical representations of logical values 0 and 1 in a way known as such. Additionally there is a SYNC line which may be set or reset to have a logical value 1 or a logical value 0 respectively. For the sake of example we will assume that a logical value 1 on the SYNC line corresponds to a frame synchronization or FSYNC signal and a logical value 0 on the SYNC line corresponds to a line synchronization or LSYNC signal. If the SYNC line does not have any definite value there is no active synchronization signal at all. The transmitting device comprises also a DATA_SEL line the role of which is described later.

The DATA line is coupled to the data input of a first differential transmitter 401 which has also an enable or select input and a differential output. Similarly the SYNC line is coupled to the data input of a second differential transmitter 403 which has also an enable or select input and a differential output. Although not separately shown in Fig. 4, the second differential transmitter 403 is dimensioned to give a higher output level than the first differential transmitter 401. The differential outputs of the differential transmitters 401 and 403 are coupled together to a differential output line consisting of lines Vline+ and Vline-. The DATA_SEL line is coupled to the enable or select input of the first differential transmitter 401 with direct polarity and to the enable or select input of the second differential transmitter 402 with reverse polarity obtained with an inverter 406.

The receiving device in Fig. 4 comprises a differential receiver 402 having a differential input, an enable or select input and an output. Additionally it comprises

a first differential amplifier 404 and a second differential amplifier 405 each having a differential input and an output. The inputs of the differential receiver 402 and the differential amplifiers 404 and 405 are all coupled to the differential input line, consisting of lines Vline+ and Vline-, of the receiving device so that the input of the second differential amplifier 405 has reverse polarity whereas the other inputs have direct polarity. The output of the differential receiver 402 is coupled to a DATA' line, the output of the first differential amplifier 404 is coupled to an FSYNC line and the output of the second differential amplifier 405 is coupled to an LSYNC line. The outputs of the first and second differential amplifiers 404 and 405 are also coupled to the enable or select input of the differential receiver 402 through a NOR gate 407.

The operation of the apparatus in Fig. 4 is illustrated in the timing diagrams of Figs. 5a and 5b. As long as the DATA_SEL line remains at logical value 1, the first differential transmitter 401 is selected and the second differential transmitter 403 is not selected, so that the logical values 1 and 0 occurring in the data bit stream to be transmitted are converted into voltage signals in the differential output line. The voltage between lines Vline+ and Vline- that is used to transmit the data bits has a certain first level, with direct and reverse polarities corresponding to the logical values 1 and 0 of the data bits respectively. When the DATA_SEL line goes into logical value 0, the first differential transmitter 401 goes into a not selected state and the second differential transmitter 403 goes into a selected state. As a result a synchronization signal is written into the differential output line. Said synchronization signal has a second voltage level that is higher than said first voltage level, and either a direct or reversed polarity according to whether the SYNC line has the logical value 1 (FSYNC) or 0 (LSYNC).

In the receiver the differential amplifiers 404 and 405 have been coupled as level indicators with a certain threshold voltage level, which is higher than said first voltage level. In other words, as long as there are only data signals coming through lines Vline+ and Vline-, the outputs of the differential amplifiers 404 and 405 remain close to zero and the DATA_EN signal remains high. This enables the differential receiver 402 to receive the data bit signals from the lines Vline+ and Vline- and to write the corresponding logical values into the DATA' line. If an FSYNC signal occurs, the first differential amplifier 404 detects it as a voltage level beyond said threshold with direct polarity, and the output of the first differential amplifier 404 goes high while the output of the second differential amplifier 405 remains low. This in turn causes the output of the NOR gate 407 to go low, which

disables the differential receiver 402. Nothing gets written into the DATA' line while the FSYNC signal is active. Similarly if an LSYNC signal occurs, the second differential amplifier 405 detects it as a voltage level beyond said threshold with reverse polarity, and the output of the second differential amplifier 405 goes high while the output of the first differential amplifier 404 remains low. This causes again the output of the NOR gate 407 to go low, which disables the differential receiver 402. Nothing gets written into the DATA' line while the LSYNC signal is active.

It is not necessary to disable the differential receiver 402 if somewhere in the other parts of the receiver circuitry it can be made clear that while either one of the synchronization signals remains active, the output on the DATA' line should be ignored. In such a case the NOR gate 407 and the connection from its output to the enable or select input of the differential receiver 402 would be superfluous.

In the embodiment of Fig. 4 the transmission of data bits must be interrupted for the time when synchronization signals are transmitted. The corresponding indefinite values of the DATA, DATA+ and DATA- lines, as well as the DATA' line in the receiver, are shown in Figs. 5a and 5b as cross-hatched time intervals. Similarly the values of the SYNC, SYNC+ and SYNC- lines are indefininte when no synchronization signals are transmitted (actually, if the differential output of the second differential transmitter 403 has a high enough impedance and the outputs of the differential transmitters 401 and 403 are not separated by e.g. diodes, the SYNC+ and SYNC- lines will follow the voltage levels of the DATA+ and DATA- lines when the SYNC line is indefinite).

Fig. 6 illustrates an alternative embodiment of the invention which is a variation of the embodiment of Fig. 4. The second differential transmitter has been replaced with a pair of parallel tri-state bus drivers 601 and 602 so that the SYNC line is coupled to the data input of both tri-state bus drivers 601 and 602, the output of the inverter 307 used to reverse the polarity of the DATA_SEL signal is coupled to the enable or select input of both tri-state bus drivers 601 and 602. The output of the first tri-state bus driver 601 is coupled to the Vline+ line and the output of the second tri-state bus driver 602 is coupled to the Vline- line. A tri-state bus driver is a known circuit element which accepts logical levels as input signals and is capable of driving a wired output connection into one of two logical voltage levels correspondingly. When a tri-state bus driver is not selected, its output is at a high impedance state. In

Fig. 6 we assume that the output levels of the first differential transmitter 401 are lower than the output levels of the tri-state bus drivers 601 and 602.

The transmitter side in Fig. 6 works otherwise in the same way as that in Fig. 4, but when the DATA_SEL signal goes low, the parallel tri-state bus drivers 601 and 602 couple the same voltage level into the Vline+ and Vline- lines and not opposite levels like the output of a differential transmitter. Taken our previous assumption that a logical 1 on the SYNC line means an FSYNC signal and a logical 0 means an LSYNC signal, an FSYNC signal is transmitted through the Vline+ and Vline- lines by setting both to the same relatively high voltage level, and an LSYNC signal is transmitted through the Vline+ and Vline- lines by setting both to the same relatively low voltage level.

On the receiver side of Fig. 6 the differential amplifiers or level indicators of Fig. 4 have been replaced by an AND gate 604 and a NOR gate 605. The outputs of these gates are coupled to the FSYNC and LSYNC lines respectively, and also to the enable or select input of the differential receiver 402 through the NOR gate 407. The idea of operation on the receiver side is the same as before: as long as the differential voltage levels used to transmit the data bits over the Vline+ and Vline- lines remain somewhere between the more extreme levels used for the FSYNC and LSYNC signals, the outputs of the logical gates 604 and 605 remain low and the DATA_EN signal remains high. When either one of the more extreme levels occurs, this time simultaneously in both lines Vline+ and Vline-, the output of the appropriate one of the logical gates 604 or 605 goes high, disabling the reception of data by setting the DATA_EN signal low through gate 407, and indicating the respective synchronization signal on the corresponding one of the FSYNC and LSYNC lines. In the timing diagram of Fig. 7a and 7b cross-hatched time intervals again denote those moments when the value of the corresponding signal is indefinite.

If we compare the embodiments of Figs. 4 an 6, the one in Fig. 4 is more advantageous in the sense that all signals in the Vline+ and Vline- lines have differential form, reducing the susceptibility to EMI: the high simultaneous voltage levels used in the embodiment of Fig. 6 both increase the interference radiated to the surroundings and make the transmission of the synchronization signals susceptible to common-more interference. However, the embodiment in Fig. 6 makes use of very commonplace and readily available parallel tri-state bus drivers instead of a

differential transmitter dimensioned for relatively high output voltage, which may reduce production costs and energy consumption.

Both embodiments shown in Figs. 4 and 6 share the slight drawback that the transmission of data must be interrupted when a synchronization signal is transmitted. This drawback is not nearly as severe as in prior art solutions, since only one bit period from the transmission per one smallest data unit (line) between consecutive synchronization signals needs to be received. However, the invention enables even continuous transmission of data as will be disclosed in the following description of Figs. 8 to 11.

Fig. 8 illustrates an arrangement where the transmitting device comprises a DATA line and a SYNC line exactly as in Figs. 4 and 6. There is also a third line, but this time it is called SYNC_EN. The first differential transmitter 401 does not have a coupling between said third line and its enable or select input. The SYNC_EN line is coupled directly to the enable or select input of the second differential transmitter 403, which is again dimensioned for higher output levels than the first differential transmitter 401. This time the output level of the second differential transmitter 403 must be higher than two times the output level of the first differential transmitter 401 for reasons described in more detail below. The outputs of the differential transmitters 401 and 403 are coupled to the differential transmission output, consisting of lines Vline+ and Vline-, through summing means so that the voltage of Vline+ will be the sum of voltages of DATA+ and SYNC+, and the voltage of Vline- will be the sum of voltages of DATA- and SYNC-.

In the receiving device there is a parallel receiver arrangement consisting of a differential receiver 801 as well as four parallel differential amplifiers 802, 803, 804 and 805 coupled as level indicators. All these are coupled to the differential transmission input consisting of lines Vline+ and Vline-. The first two differential amplifiers 802 and 803 are coupled to the lines Vline+ and Vline- with direct polarity and the other two differential amplifiers 804 and 805 are coupled to the lines Vline+ and Vline- with reverse polarity. Although not specifically shown in Fig. 8, the relative sensitivities of the differential amplifiers 802 to 805 are selected so that the first and third differential amplifiers 802 and 804 indicate when a differential input signal exceeds a certain first threshold level and the second and fourth differential amplifiers 803 and 805 indicate when a differential input signal exceeds a certain second threshold level which is higher than said first threshold level.

The output of the first differential amplifier 802 is coupled to an FSYNC line and the output of the third differential amplifier 804 is coupled to an LSYNC line. The outputs of the second and fourth differential amplifiers 803 and 805 are coupled to inverters 806 and 809 respectively. The outputs of the first differential amplifier 802 and the first inverter 806 are coupled to a first AND gate 807, and the outputs of the third differential amplifier 804 and the second inverter 809 are coupled to a second AND gate 810. The outputs of the first and second AND gates 807 and 810 are coupled to an OR gate 808. The outputs of the differential receiver 801 and the OR gate 808 are coupled to an exclusive-OR or XOR gate 811, the output of which is coupled to a DATA' line.

In the transmitting device the first differential transmitter 401 transmits continuously a stream of data bits into its differential output consisting of lines DATA+ and DATA-. As long as the SYNC_EN signal remains low, the second differential transmitter 403 is not selected and the voltage in the SYNC+ and SYNC- lines is zero, meaning that the Vline+ and Vline- lines follow the voltages of the DATA+ and DATA- lines respectively. When the SYNC_EN signal goes high, the second differential transmitter 403 sets the voltages of the SYNC+ and SYNC- lines according to the current signal value on the SYNC line. We may again assume that an FSYNC signal corresponds to a high value on the SYNC line and an LSYNC signal corresponds to a low value on the SYNC line.

Let us analyze more carefully the voltages of the Vline+ and Vline- lines depending on the value combinations on the DATA, SYNC and SYNC_EN lines. We may use a notation according to which the output of the first differential transmitter 401 is from -Vth1 to +Vth1. As described above, if the SYNC_EN signal is low, these are also the voltages of the Vline+ and Vline- lines. Taken that the second differential transmitter 403 is dimensioned to give a higher output voltage level than two times that of the first differential transmitter 401, we may note that e.g. if DATA is low and SYNC and SYNC_EN both are high, then the voltage of Vline+ is equal to some +Vth2, which is higher than said +Vth1, and the voltage of Vline- is equal to some -Vth2, which is lower than said -Vth1. If DATA, SYNC and SYNC_EN are all high, then the voltage of Vline+ is equal to some +Vth3, which is even higher than said +Vth2, and the voltage of Vline- is equal to some -Vth3, which is even lower than said -Vth2. For completeness we may show all possible combinations in the following table.

	DATA	SYNC	SYNC_EN	Vline+	Vline-
DATA high, no SYNC	1	X	0	+Vth1	-Vth1
DATA low, no SYNC	0	X	0	-Vth1	+Vth1
DATA high, FSYNC	1	1	1	+Vth3	-Vth3
DATA low, FSYNC	0	1	1	+Vth2	-Vth2
DATA high, LSYNC	1	0	1	-Vth2	+Vth2
DATA low, LSYNC	0	0	1	-Vth3	+Vth3

These signal combinations and voltage levels are also shown in Fig. 9a.

In the receiving device the first differential amplifier 802 is arranged to detect a positive voltage difference equal to or greater than +Vth2...-Vth2 in the differential input line: the presence of such a positive voltage difference indicates an FSYNC signal. Simultaneously with the FSYNC signal there may come a data bit that is either 1 or 0, and the receiver must be able to distiguish between these cases. Therefore the second differential amplifier 803 is arranged to detect a positive voltage difference equal to +Vth3...-Vth3 in the differential input line. If such a positive voltage difference is present, the simultaneous data bit is 1. If, however, such a large positive voltage difference is not present, the simultaneous data bit is 0. The circuit consisting of the first inverter 806, the first AND gate 807 and the OR gate 808 is designed to give a 1 to the second input of the XOR gate 811 if the detected positive voltage difference is equal to or greater than +Vth2....-Vth2, but not as large as +Vth3...-Vth3 so that in that case the 1 given by the differential receiver 801 is inverted to 0 before writing it into the DATA' line. A similar deduction concerning the parts 804, 805, 809, 810 and 808 leads to the result that LSYNC is indicated every time when a negative voltage difference equal to or greater than -Vth2...+Vth2 is detected in the differential input line, and the 0 given by the differential receiver 801 is inverted to 1 before writing it into the DATA' line if the negative voltage difference is not as large as -Vth3...+Vth3.

Figs. 9b and 9c present a timing diagram where the difference between the second and last LSYNC pulses illustrate the inverting function implemented with parts 804, 805, 809, 810, 808 and 811.

Fig. 10 illustrates an embodiment of the invention which is altenative to that of Fig. 8. The transmitting device is equal, but the arrangement of parallel differential receivers and amplifiers in the receiving device as well as the associated logic

circuitry have been replaced with a three-bit analogue to digital converter 1001 and a logic block 1002. Fig. 11 illustrates an examplary way how a voltage scale from below -Vth3' to above +Vth3' can be arranged into discrete voltage ranges: the lowest range, below -Vth3', is mapped into bit combination 0,0,0; the next lowest into bit combination 0,0,1; and so on until the highest voltage range, over +Vth3', is mapped into bit combination 1,1,1. Note that the primed threshold voltage values are twice as large as the previously used unprimed ones, since the differential input of the analogue to digital converter is floating and no reference to zero or ground potential is used. In order to produce the correct combinations of DATA', FSYNC and LSYNC signals from the indicated analog to digital mappings the logic block 1002 must do the conversions shown in the following table.

Output of A/D converter	Output of logic block (DATA', FSYNC, LSYNC)
0,0,0	0,0,1
0,0,1	0,0,1
0,1,0	1,0,1
0,1,1	0,0,0
1,0,0	1,0,0
1,0,1	0,1,0
1,1,0	1,1,0
1,1,1	1,1,0

It is obvious as such for a person skilled in the art to construct the logic block 1002 so that it does the required conversions.

It is naturally possible to use the parallel tri-state bus driver solution shown in Fig. 6 also in the embodiments shown in Figs. 8 and 10, with approximately the same influence to the advantageous and disadvantageous effects that have to be taken into consideration. Based on the above-given teachings it is obvious for a person skilled in the art how the detection arrangement in the receiving device must be modified if the synchronization signals come as equal voltage levels on both lines Vline+ and Vline- instead of voltage levels having opposite polarities. In the embodiments shown in Figs. 8 and 10 another possible modification of the invention is the one where the synchronization signals are set for a longer time than one bit period. This would not only reduce the risk of a synchronization signal going unnoticed because of a sudden and short communication error, but it would also give the possibility to

transmit several different synchronization and/or other control signals that differ from each other by their duration in time. The receiving device should in such a case have a counter that would count the length in bit periods of each received synchronization signal and map the counted lengths into appropriate different synchronization indications.

In the described embodiments we have only used two synchronization signals, namely FSYNC and LSYNC. However, the invention is not limited to the use of two synchronization signals, because each additional pair of synchronization signals can be accommodated by providing an additional differential transmitter (or parallel tri-state bus driver pair) in the transmitting device and an additional detection arrangement obtained from the described embodiments by obvious extrapolation in the receiving device. Instead of using separate differential transmitters for all signals that require different signal levels it would be possible to use a single controllable differential transmitter the amplification factor of which could be set separately for each type of signal to be transmitted.

The invention reduces the risk of losing synchronization, because even if a cycle or even a number of cycles from a data bit sequence between synchronization signals is lost, the detection of the next synchronization signal will succeed because it is completely independent of the detection of data bits. For the receiver it suffices to monitor the signal levels and to detect the next occurrence of a signal level that is not one of the usual data signal levels to achieve synchronization. Although we have described only embodiments where the synchronization signals are transmitted generally on higher signal levels than the data bits, it is perfectly possible to switch the roles of the levels so that the data bits are transmitted on a higher level than the synchronization signals. However, because there are much more data bits than synchronization signals to be transmitted, it is usually more advantageous to use the lower signal levels for the data bits since this helps to reduce energy consumption and EMI originating at the serial interface.

Fig. 12 illustrates the use of an arrangement according to Fig. 4, 6, 8 or 10 as a comparison to Fig. 2a where a prior art arrangement was described. The serial interface arrangement according to the invention is generally represented by block 1200. There is an additional logic block 1201 the function of which is to map the LSYNC and FSYNC signals given by the data originator 201 into SYNC and DATA_SEL or SYNC_EN signals: the mapping is easily done since DATA_SEL must remain high and SYNC must remain indefinite as long as LSYNC and FSYNC

are low, and when one of LSYNC and FSYNC is high DATA_SEL must go low and SYNC must be either high or low depending on which one of LSYNC and FSYNC is high. If SYNC_EN is used instead, it must be low as long as LSYNC and FSYNC are low and high otherwise. The logic circuit that fulfils these functions only needs to comprise a couple of basic ports.

The clock signal multiplier and divider blocks 203' and 204' deserve some additional attention. In those embodiments of the invention where a synchronization signal replaces the transmission of data bits the clocking arrangement must take into account the fact that the transmission frequency is not an exact multiple of the parallel data processing frequency by the number of parallel data lines. Either the clock signal must be interrupted for the duration of a synchronization signal to be transmitted or the multiplier / divider number must be variable or so selected that the synchronization signals can be accommodated between the transmitted data bits without the parallel to serial and serial to parallel conversions either running ahead of the serial transmission pace or lagging behind it. In those embodiments of the invention where the synchronization signals are superimposed with data bits the clock frequency for the parallel to serial and serial to parallel conversions is simply the multiple of the parallel data processing frequency by the number of parallel data lines.

If the invention is applied to a portable terminal of a telecommunication system, the transmitting device 201 may be e.g. a camera, in which case the receiving device 202 may be e.g. a frame memory. Or the transmitting device 201 may be a frame memory and the receiving device 202 may be a display.

CLAIMS

1. A digital transmitting device for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising:
- primary transmitter means for converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels and
- secondary transmitter means for converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

2. A digital transmitting device according to claim 1, comprising means for disabling the output of data signal levels into said output line for the time of outputting synchronization signal levels into said output line.

3. A digital transmitting device according to claim 2, wherein
- said primary transmitter means comprise a first transmitter having a data input, an output and an enable or select input,
- said secondary transmitter means comprise a second transmitter having a data input, an output and an enable or select input,
- the digital transmitting device comprises a selection signal line and
- said selection signal line is coupled to the enable or select input of said first transmitter with direct polarity and to the enable or select input of said second transmitter with reverse polarity.

4. A digital transmitting device according to claim 2, wherein
- said primary transmitter means and said secondary transmitter means are implemented as complementary modes of a single controllable transmitter having a control input to control its amplification factor,
- the digital transmitting device comprises a control signal line and
- said control signal line is coupled to the control input of said single controllable transmitter.

5. A digital transmitting device according to claim 1, comprising means for summing the outputs of said primary transmitter means and said secondary transmitter means into combined output levels in said output line.

6. A digital transmitting device according to claim 1, wherein
- said output line is a differential wired connection consisting of a first signal line and a second signal line, and
- said primary transmitter means is a low-voltage level differential transmitter.

7. A digital transmitting device according to claim 6, wherein said secondary transmitter means is a differential transmitter having differential output levels that are remarkably farther from zero than the output levels of said low-voltage level differential transmitter.

8. A digital transmitting device according to claim 6, wherein said secondary transmitter means comprises a pair of parallel tri-state bus drivers having non-differential output levels that are remarkably farther from zero than the output levels of said low-voltage level differential transmitter.

9. A digital receiving device for receiving a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising:
- primary receiver means, responsive to a first group of signal levels, for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits and
- secondary receiver means, responsive to a second group of signal levels which consists of different levels than said first group of signal levels, for converting synchronization signal levels in said input line into synchronization signals.

10. A digital receiving device according to claim 9, wherein
- said primary receiver means is a low-voltage level differential receiver responsive to voltage signals at a certain first distance from zero,
- said secondary receiver means comprises two parallel differential amplifiers coupled as level indicators to said input line with opposite polarities and responsive to voltage signals at a certain second distance from zero, which is larger than said first distance.

11. A digital receiving device according to claim 10, comprising:
- an enable or select input in said low-voltage level differential receiver and
- a coupling from the outputs of said parallel differential amplifiers to said enable or select input arranged to disable said low-voltage level differential receiver as a

response to an affirmative level indication from either one of said parallel differential amplifiers.

12. A digital receiving device according to claim 10, wherein
- said secondary receiver means comprises also two other parallel differential amplifiers coupled as level indicators to said input line with opposite polarities and responsive to voltage signals at a certain third distance from zero, which is larger than said second distance,
- said four parallel differential amplifiers constitute two differential amplifier pairs so that in each pair the differential amplifiers are coupled as level indicators to said input line with same polarity but responsive to voltage signals at a different distance from zero,
- the digital receiving device comprises additionally inverting means for conditionally inverting the output of said low-voltage level differential receiver as a response to a certain indication and
- from each differential amplifier pair there is a coupling to said inverting means for producing said indication as a response to a situation where exactly one of the amplifiers in the differential amplifier pair gives an affirmative level indication.

13. A digital receiving device according to claim 9, wherein said primary receiver means and said secondary receiver means are implemented within a mapping entity arranged to map a number of input signal levels into corresponding bit combinations where the reception of signal levels belonging to said first group of signal levels corresponds to different bit combinations than the reception of signal levels belonging to said second group of signal levels.

14. A digital receiving device according to claim 13, wherein said mapping entity consists of an analog to digital converter and an associated logic block.

15. An electronic device comprising a first circuit element and a second circuit element for processing digital image data consisting of data sequences and synchronization signals, comprising:
- within the first circuit element a digital transmitting device for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, said digital transmitting device comprising:
    - primary transmitter means for converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels and

- secondary transmitter means for converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels; and

- within the second circuit element a digital receiving device for receiving a serial sequence of data bits and a number of associated synchronization signals over a wired connection, said digital receiving device comprising:

- primary receiver means, responsive to a first group of signal levels, for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits and

- secondary receiver means, responsive to a second group of signal levels which consists of different levels than said first group of signal levels, for converting synchronization signal levels in said input line into synchronization signals.

16. A method for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising the steps of:

- converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels, and

- converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

17. A method according to claim 16, wherein, as a part of the step of converting synchronization signals into synchronization signal levels on said output line, the simultaneous conversion of data bits into successive data signal levels in said output line is disabled so that synchronization signal levels and data signal levels only occur alone in said output line.

18. A method according to claim 16, wherein, as a part of the step of converting synchronization signals into synchronization signal levels on said output line, the simultaneous conversion of data bits into successive data signal levels in said output line is upheld so that synchronization signal levels and data signal levels occur in superposition in said output line.

Abstract

A digital serial interface is provided between a transmitting device (303) and a receiving device (304) for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection. The transmitting device comprises primary transmitter means (401) for converting a serial sequence of data bits into successive data signal levels in an output line (Vline+, Vline-). Said data signal levels are selected from a first group of levels. The transmitting device comprises also secondary transmitter means (403, 601, 602) for converting synchronization signals into synchronization signal levels on said output line. Said synchronization signal levels are selected from a second group of levels which consists of different levels than said first group of levels. The receiving device comprises primary receiver means (402, 801) that are responsive to a first group of signal levels. They are used for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits. The receiving device comprises also secondary receiver means (404, 405, 802, 804) that are responsive to a second group of signal levels which consists of different levels than said first group of signal levels. They are used for converting synchronization signal levels in said input line into synchronization signals.

Fig. 4

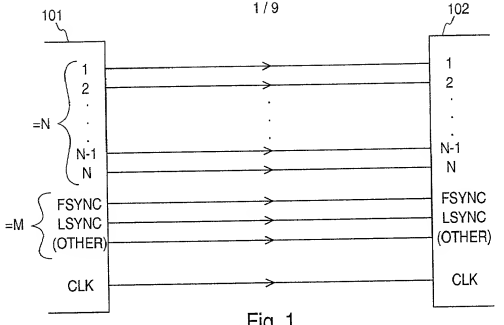


Fig. 1
PRIOR ART

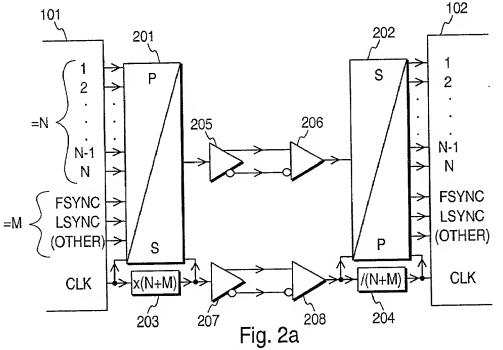


Fig. 2a
PRIOR ART

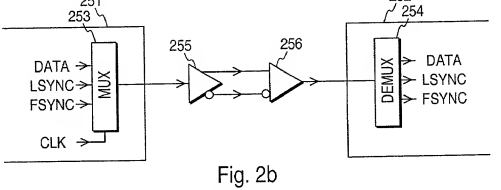


Fig. 2b
PRIOR ART

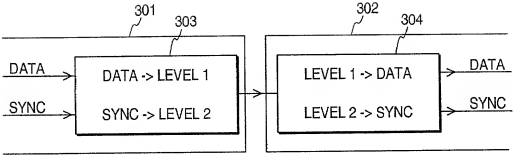


Fig. 3

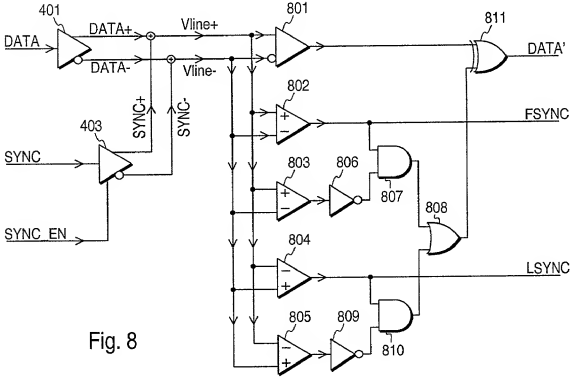


Fig. 8

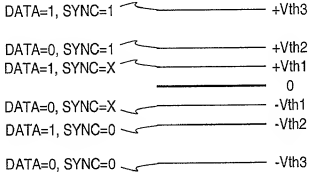


Fig. 9a

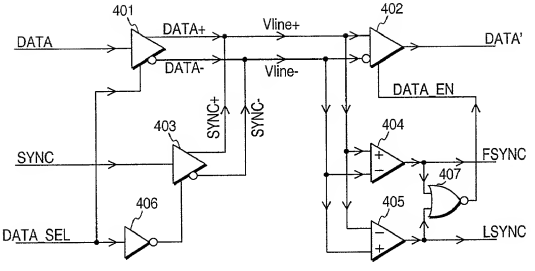

401
DATA
DATA+
DATA-
Vline+
Vline-
402
DATA'
DATA_EN
403
SYNC+
SYNC-
SYNC
404
FSYNC
407
405
LSYNC
406
DATA_SEL

Fig. 4

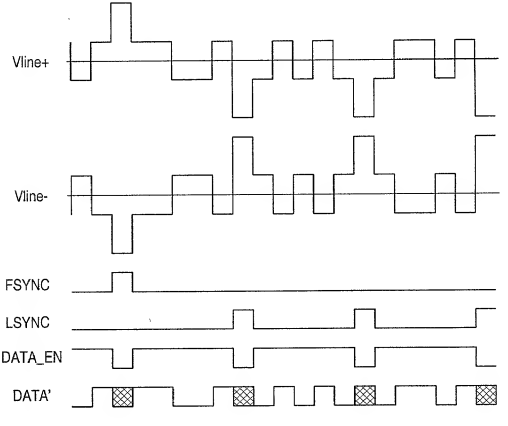

Vline+
Vline-
FSYNC
LSYNC
DATA_EN
DATA'

Fig. 5b

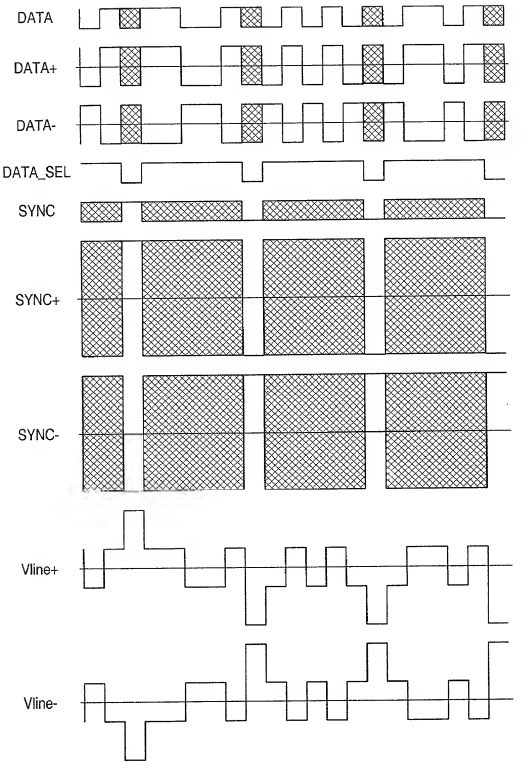


Fig. 5a

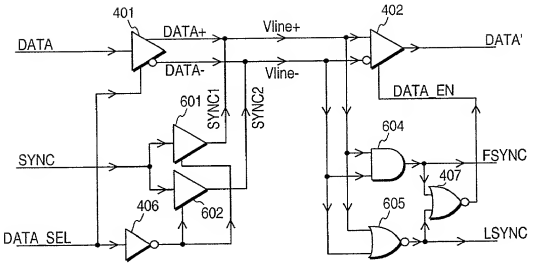

401
DATA
DATA+
DATA-
Vline+
Vline-
402
DATA'
DATA_EN
601
SYNC1
SYNC2
SYNC
604
FSYNC
407
406
602
605
DATA_SEL
LSYNC

Fig. 6

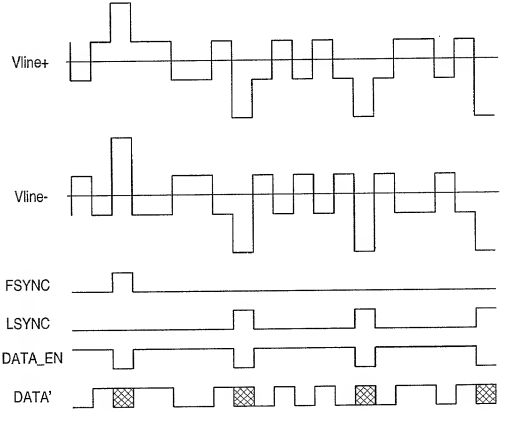

Vline+
Vline-
FSYNC
LSYNC
DATA_EN
DATA'

Fig. 7b

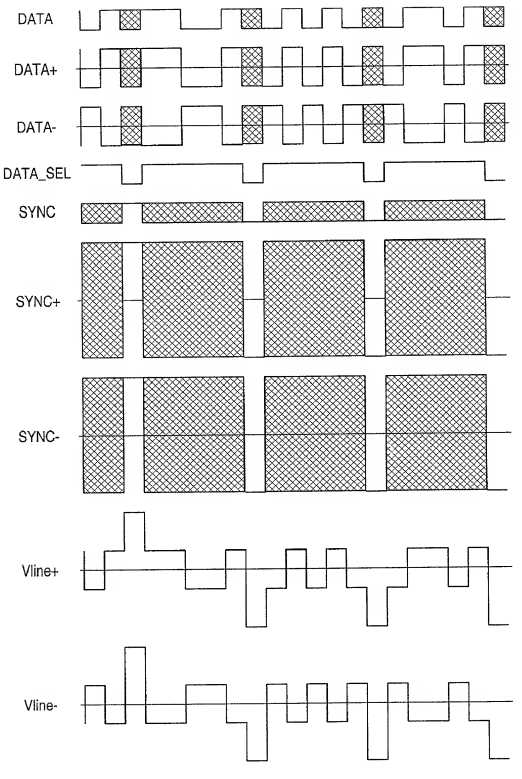


Fig. 7a

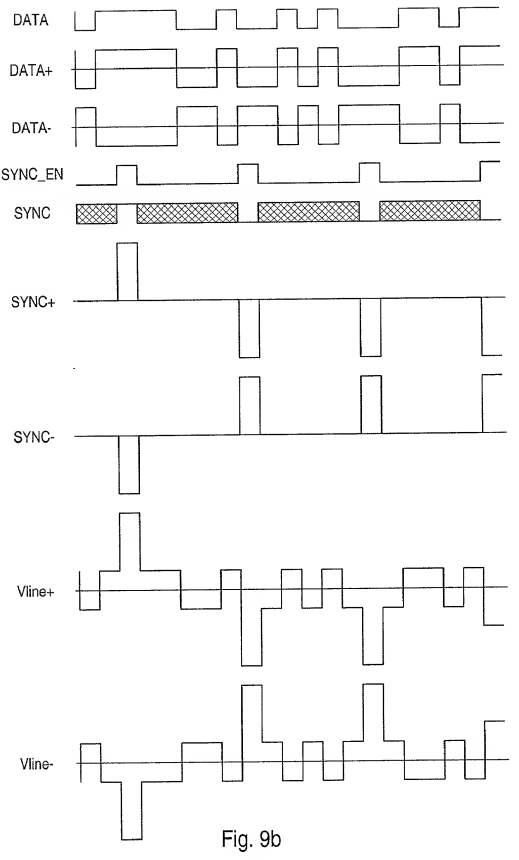


Fig. 9b

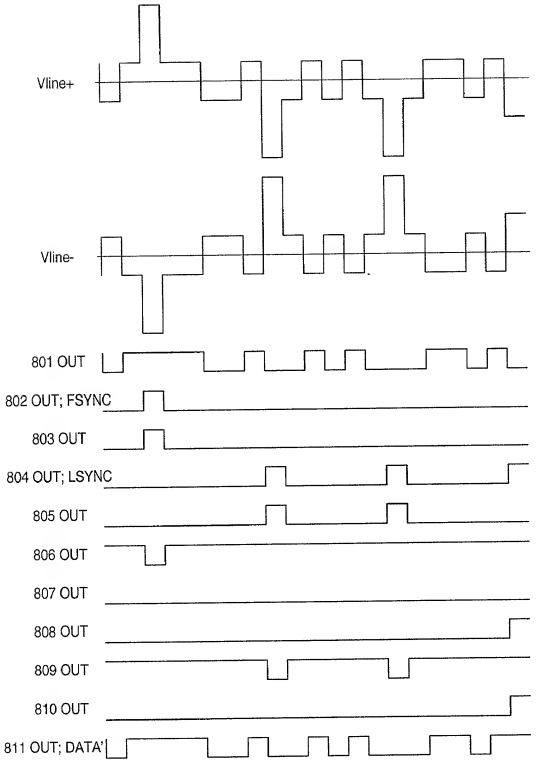

Vline+
Vline-
801 OUT
802 OUT; FSYNC
803 OUT
804 OUT; LSYNC
805 OUT
806 OUT
807 OUT
808 OUT
809 OUT
810 OUT
811 OUT; DATA'

Fig. 9c

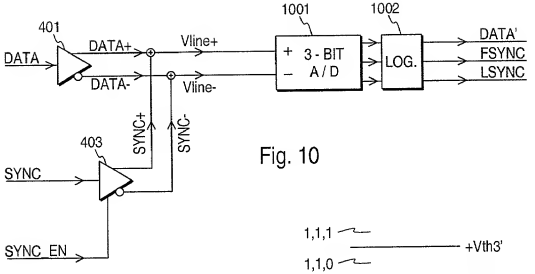


Fig. 10

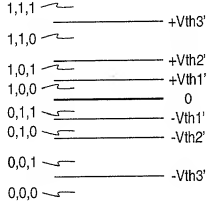


Fig. 11

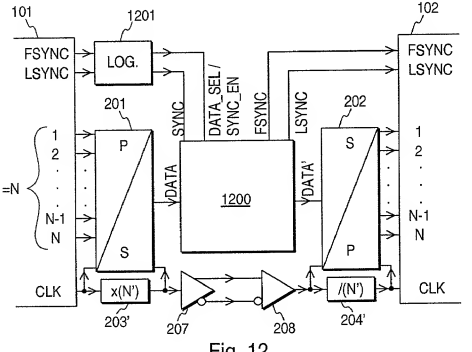


Fig. 12

Attorney's Docket No. _____ **PATENT**

COMBINED DECLARATION AND POWER OF ATTORNEY
(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type:

(check one applicable item below)

X original.
__ design.
__ supplemental.

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.

__ national stage of PCT.

NOTE: If one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR C-I-P.

__ divisional.
__ continuation.
__ continuation-in-part (C-I-P).

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims, an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

Serial interface and method for transferring digital data over a serial interface

SPECIFICATION IDENTIFICATION

the specification of which:

(complete (a), (b) or (c))

(a) X is attached hereto.

(b) __ was filed on _____, as Serial No _____
or __ Express Mail No., as Serial No. not yet known _____
and was amended on_____*(if applicable)*.

NOTE: Amendments filed after the original papers are deposited with the PTO that contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) __ was described and claimed in PCT International Application No._____,
filed on _____ and as amended under PCT Article 19 on
_____ *(if any)*.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56,

(also check the following items, if desired)

_X_ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

__ in compliance with this duty, there is attached an information disclosure statement, in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. § 119(a)-(d))

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) __ no such applications have been filed.

(e) X such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119(a)-(d)

COUNTRY(OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
FINLAND	19991900	6 September 1999	X YES NO__
			__YES NO__
			__YES NO__
			__YES NO__
			__YES NO__

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S) (34 U.S.C. § 119(e))

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

PROVISIONAL APPLICATION NUMBER	FILING DATE
_____/_____	_____
_____/_____	_____
_____/_____	_____

CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S) UNDER 35 U.S.C. 120

__ The claim for the benefit of any such applications are set forth in the attached ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CONTINUATION-IN PART (C-I-P) APPLICATION.

ALL FOREIGN APPLICATION(S), *IF ANY*, FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

_____

_____

_____

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR C-I-P APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

(list name and registration number)

Clarence A. Green	(24,622)
Harry F. Smith	(32,493)
Mark F. Harrington	(31,686)

(check the following item, if applicable)

__ Attached, as part of this declaration and power of attorney, is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO

Clarence A. Green
Perman & Green
425 Post Road
Fairfield, Ct 06430

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)

Clarence A. Green
203-259-1800

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: Carefully indicate the family (or last) name, as it should appear on the filing receipt and all other documents.

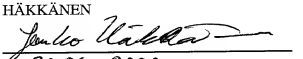
Full name of sole or first inventor:

Given name: Esa
Middle initial or name:
Family (or last name): HÄRMÄ

Inventor's signature: 
Date: 30.6.2000
Country of Citizenship: Finland
Residence: Koulumäenkatu 9, FIN-24240 SALO, Finland
Post Office Address: Koulumäenkatu 9, FIN-24240 SALO, Finland

Full name of second joint inventor, if any:

Given name: Jouko
Middle initial or name:
Family (or last name): HÄKKÄNEN

Inventor's signature: 
Date: 30.06.2000
Country of Citizenship: Finland
Residence: Ajokatu 7B, FIN-24280 SALO, Finland
Post Office Address: Ajokatu 7B, FIN-24280 SALO, Finland

Full name of third joint inventor, if any:

Given name:
Middle initial or name:
Family (or last name):

Inventor's signature: _____
Date: _____
Country of Citizenship:
Residence:
Post Office Address:

Full name of fourth joint inventor, if any:

Given name:
Middle initial or name:
Family (or last name):

Inventor's signature: _____
Date: _____
Country of Citizenship:
Residence:
Post Office Address:

(check proper box(es) for any of the following added page(s) that form a part of this declaration)

__ **Signature** for fifth and subsequent joint inventors. *Number of pages added _____.*

* * *

__ **Signature** by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added _____.*

* * *

__ **Signature** for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added _____.*

* * *

__ Added page for **signature** by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time. (37 CFR 1.47)

* * *

__ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application.
__ Number of pages added _____

* * *

__ Authorization of attorney(s) to accept and follow instructions from representative.

* * *

(if no further pages form a part of this Declaration, then end this Declaration with this page and check the following item)
_X_ This declaration ends with this page.